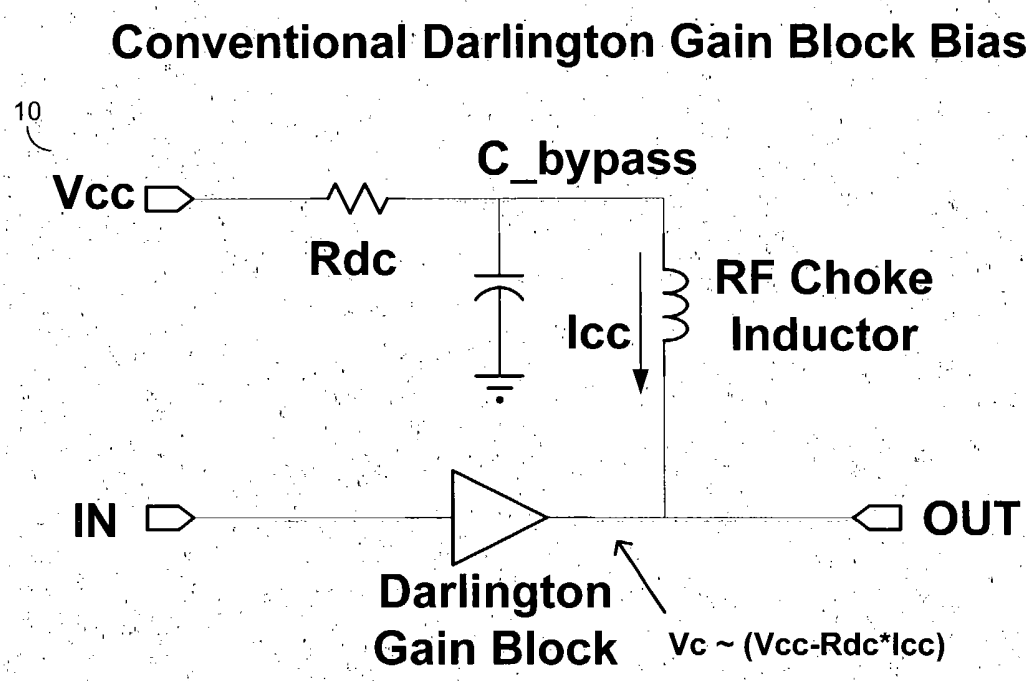

Conventional Darlington Gain Block Bias
10
Vcc
Rdc
C_bypass
Icc
RF Choke
Inductor
IN
OUT
Darlington
Gain Block
Vc ~ (Vcc-Rdc*Icc)

FIG. 1

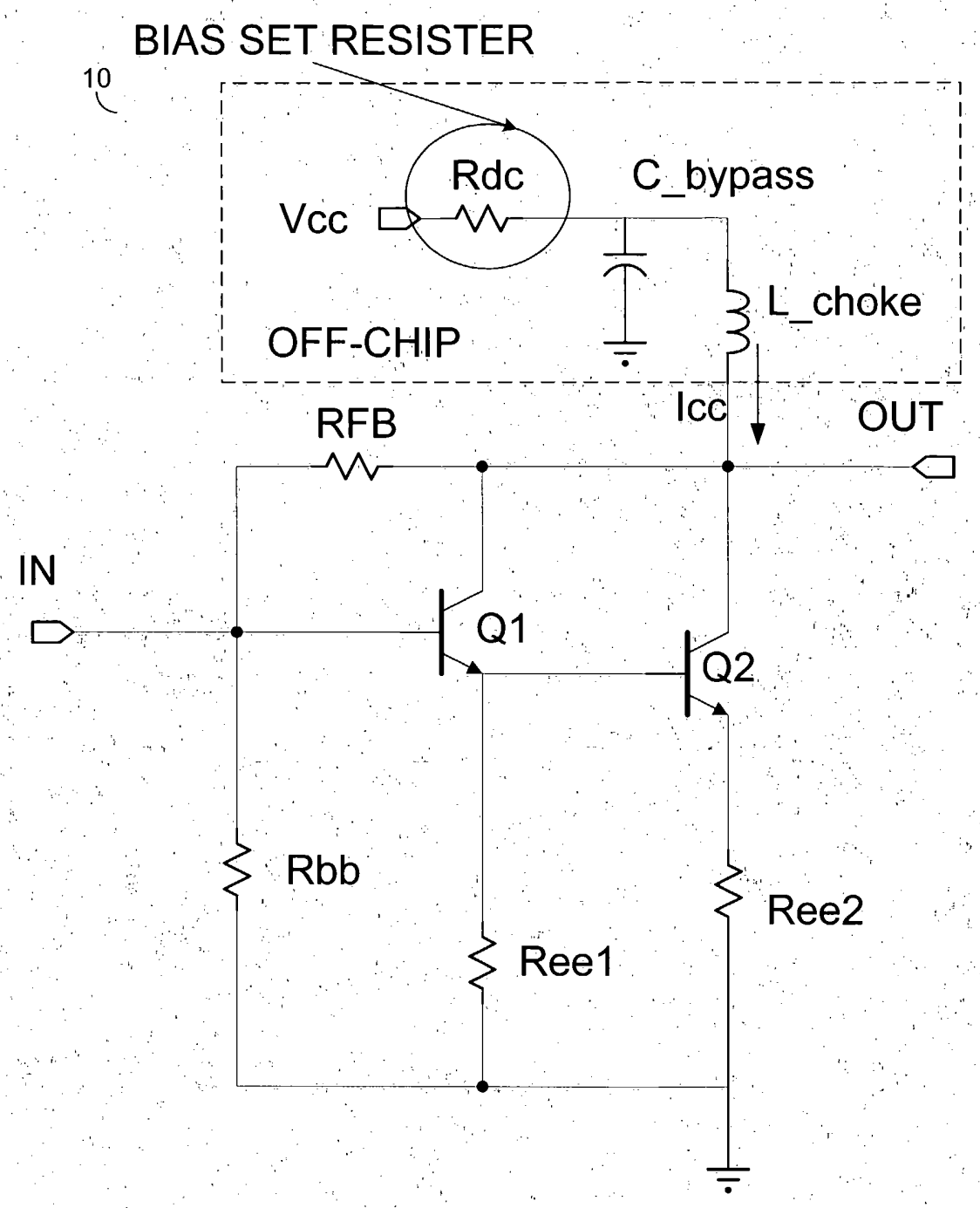
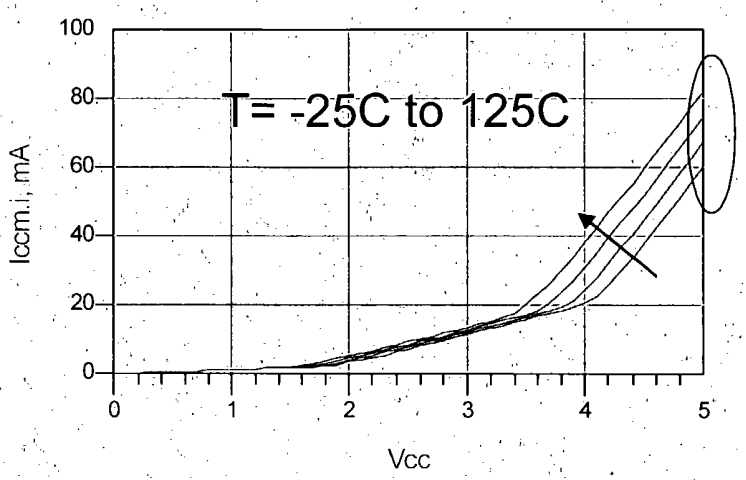

BIAS SET RESISTER
10
Rdc
C_bypass
Vcc
L_choke
OFF-CHIP
Icc
OUT
RFB
IN
Q1
Q2
Rbb
Ree2
Ree1

FIG. 2

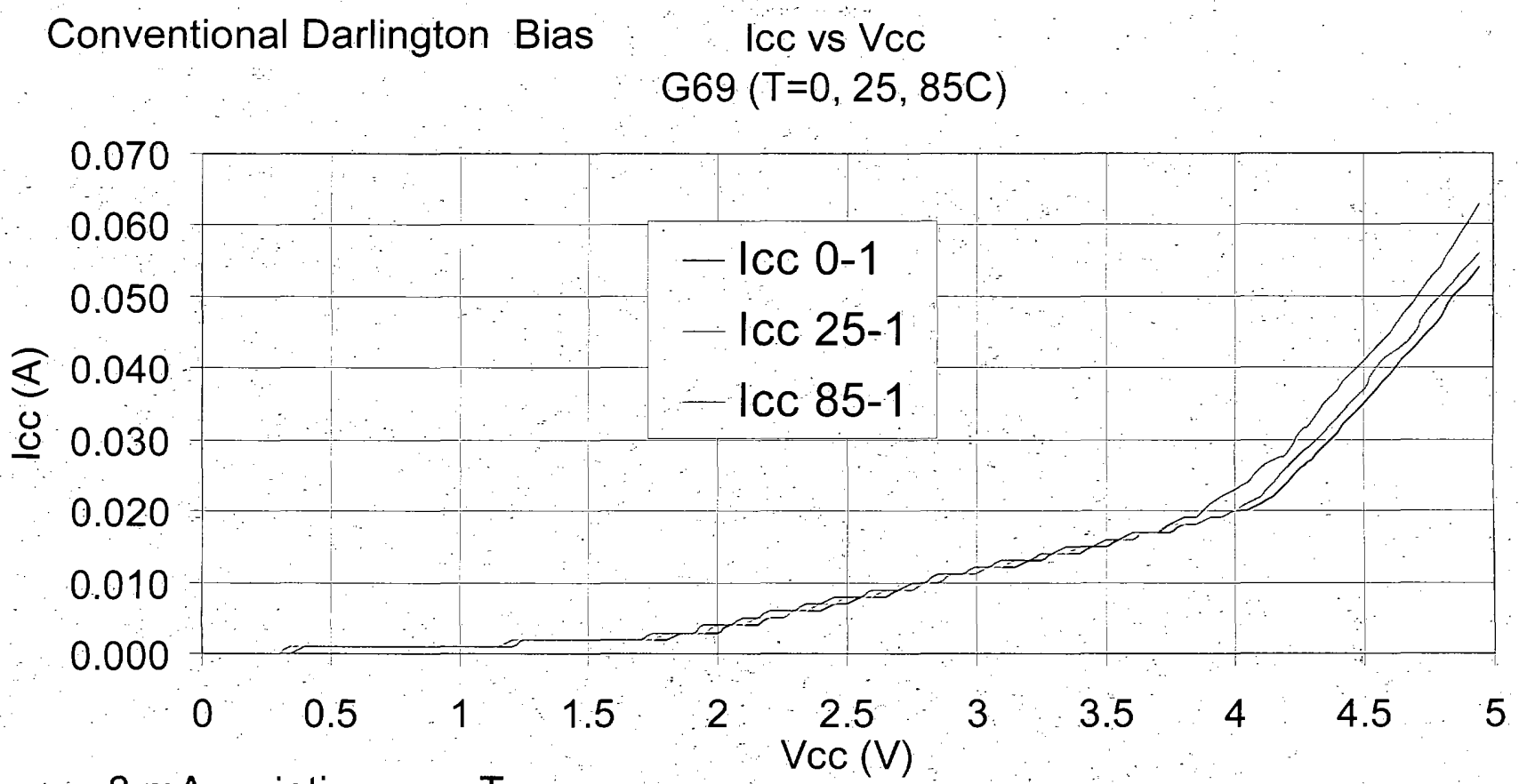
Conventional Darlington Bias



20 mA Variation or +/- 14%

FIG. 3

Conventional Darlington Bias



~8 mA variation over Temp
(13% variation, T=0-85C)
~40 mA/V Vcc sensitivity

FIG. 4

Conventional Darlington Bias

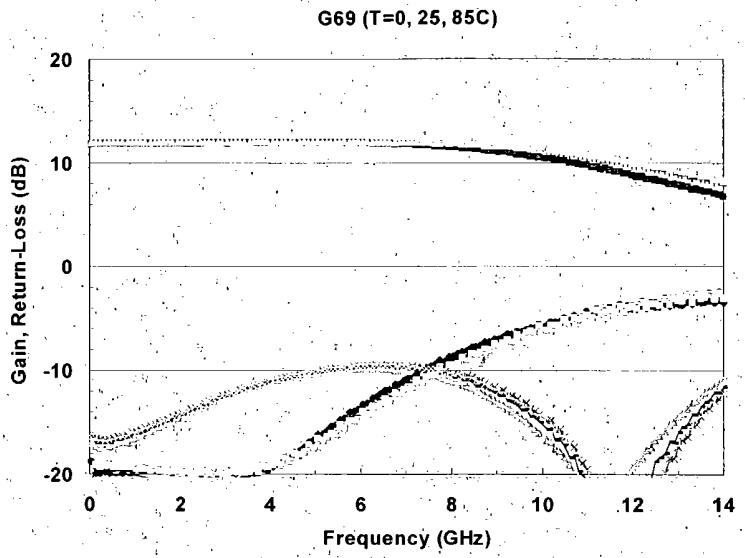


FIG. 5

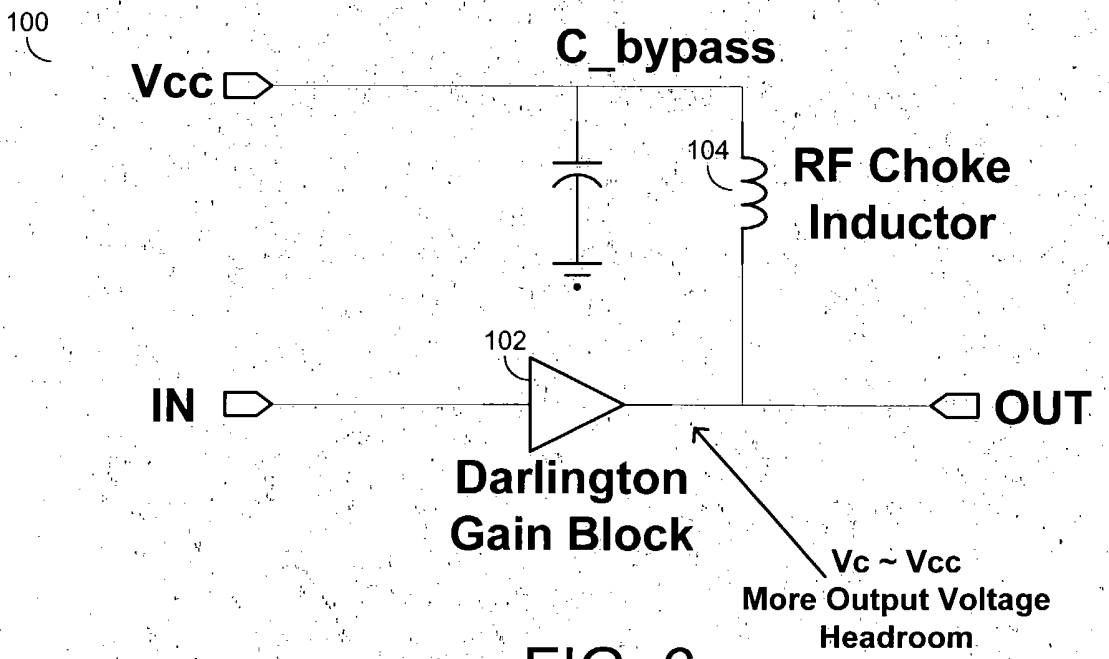


FIG. 6

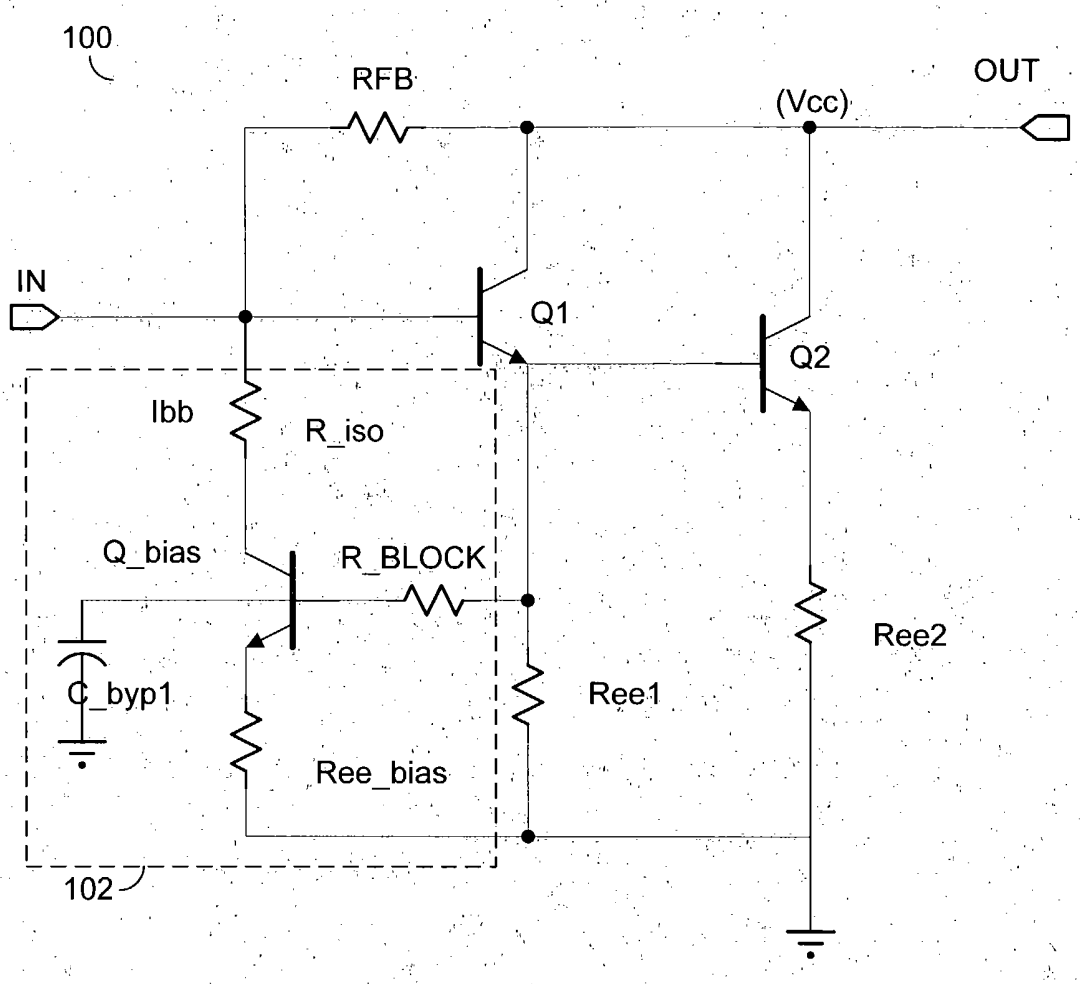
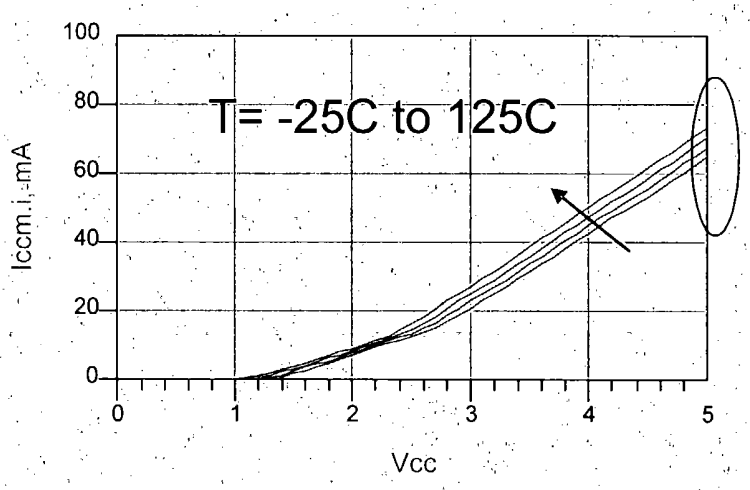

100
RFB
OUT
(Vcc)
IN
Q1
Q2
Ibb
R_iso
Q_bias
R_BLOCK
Ree2
C_byp1
Ree1
Ree_bias
102

FIG. 7



10 mA Variation or +/- 7%

FIG. 8

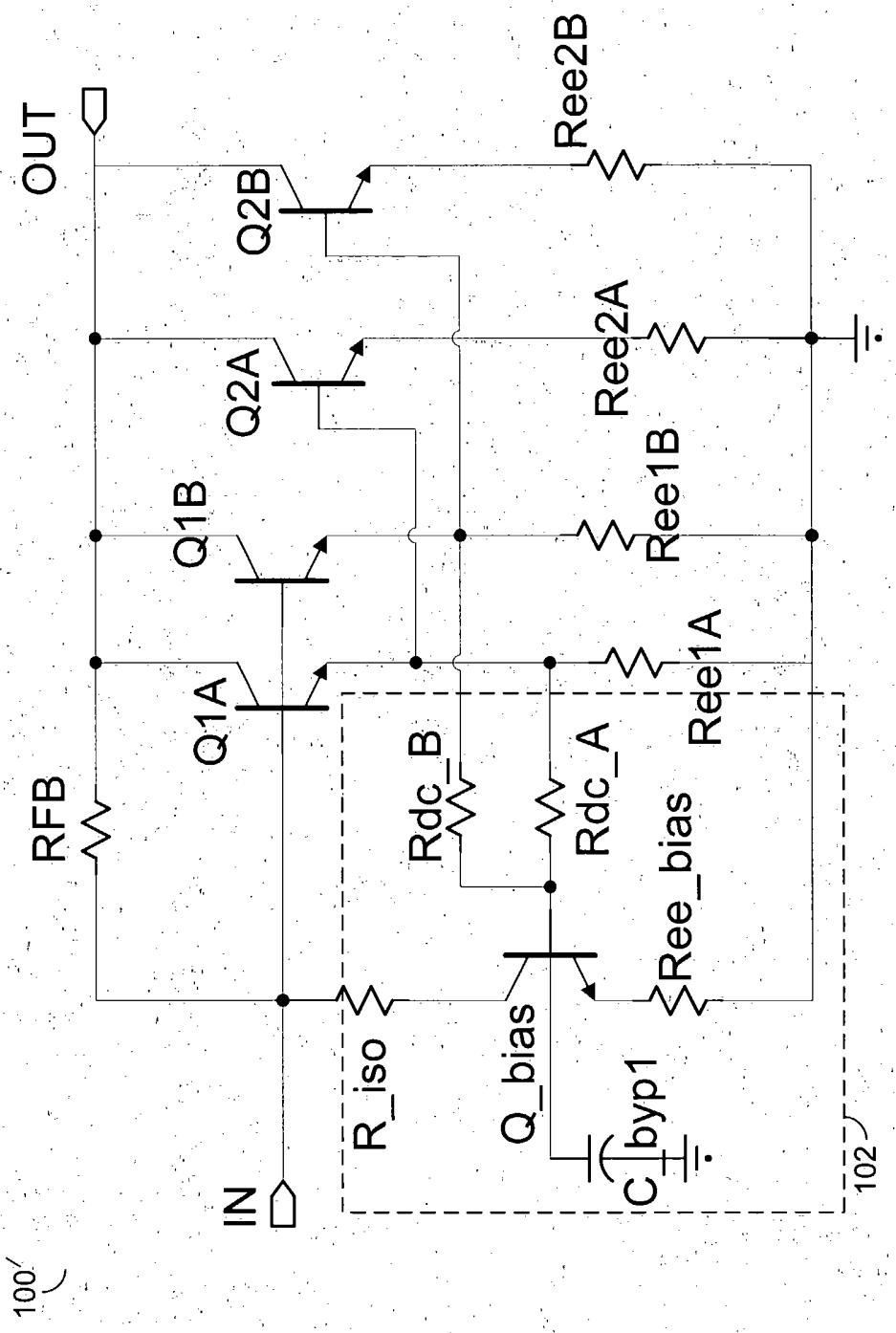

OUT
Ree2B
Q2B
Ree2A
Q2A
Q1B
Ree1B
Q1A
Ree1A
RFB
Rdc_B
Rdc_A
Ree_bias
R_iso
Q_bias
C_byp1
IN
100
102

FIG. 9

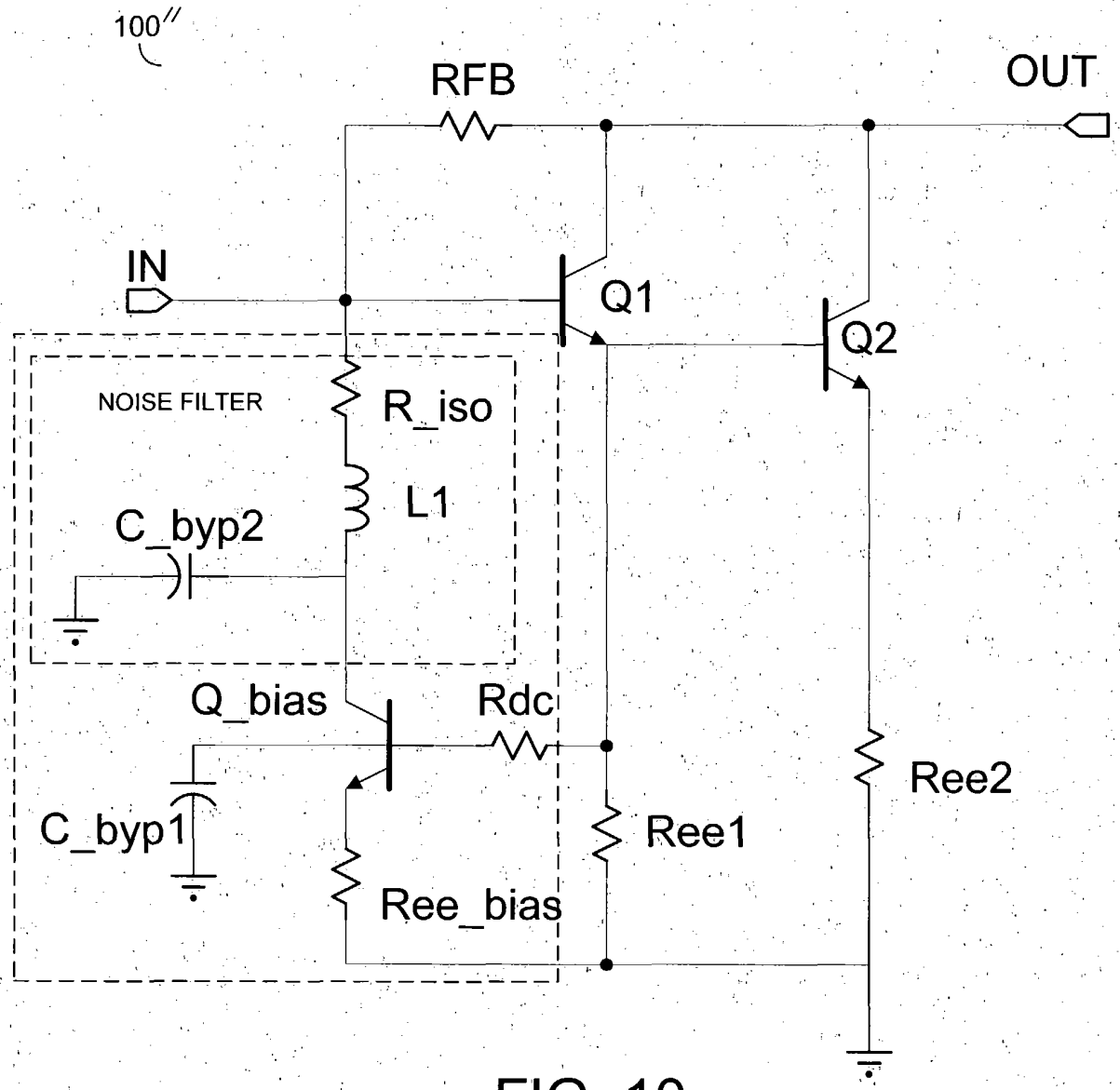

100''
RFB
OUT
IN
Q1
Q2
NOISE FILTER
R_iso
L1
C_byp2
Q_bias
Rdc
C_byp1
Ree1
Ree2
Ree_bias

FIG. 10

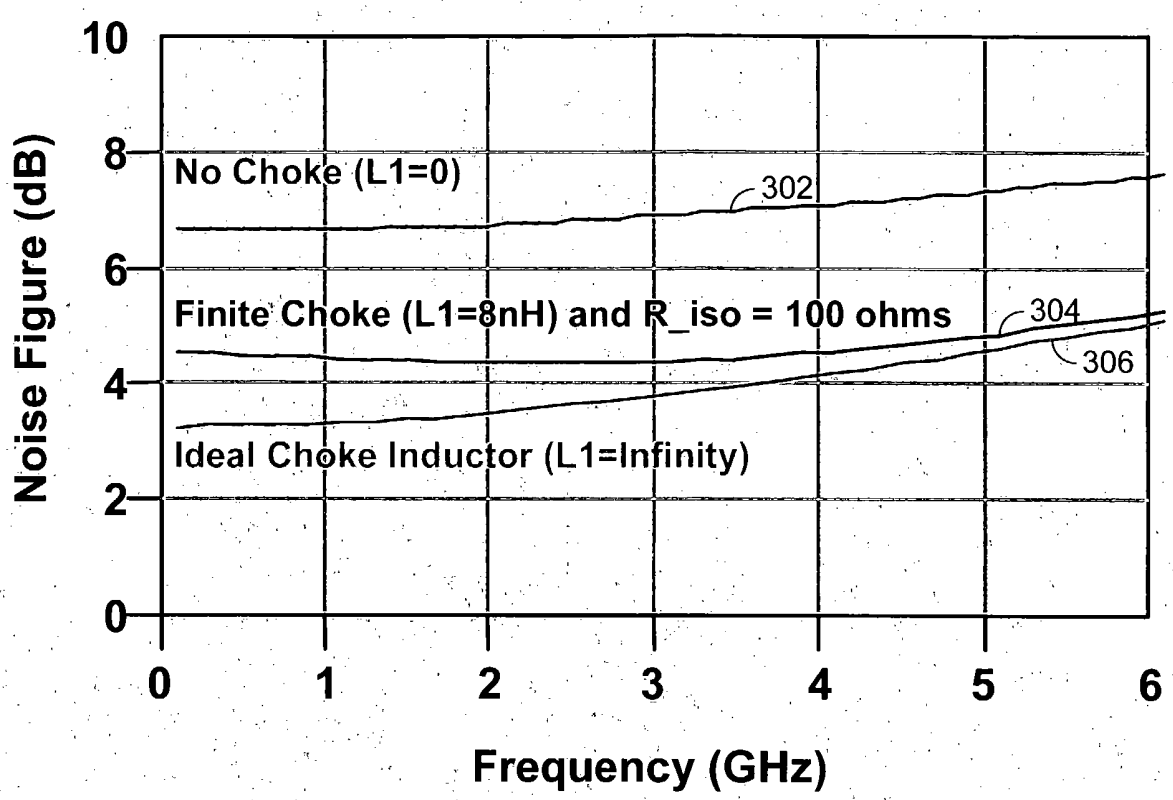
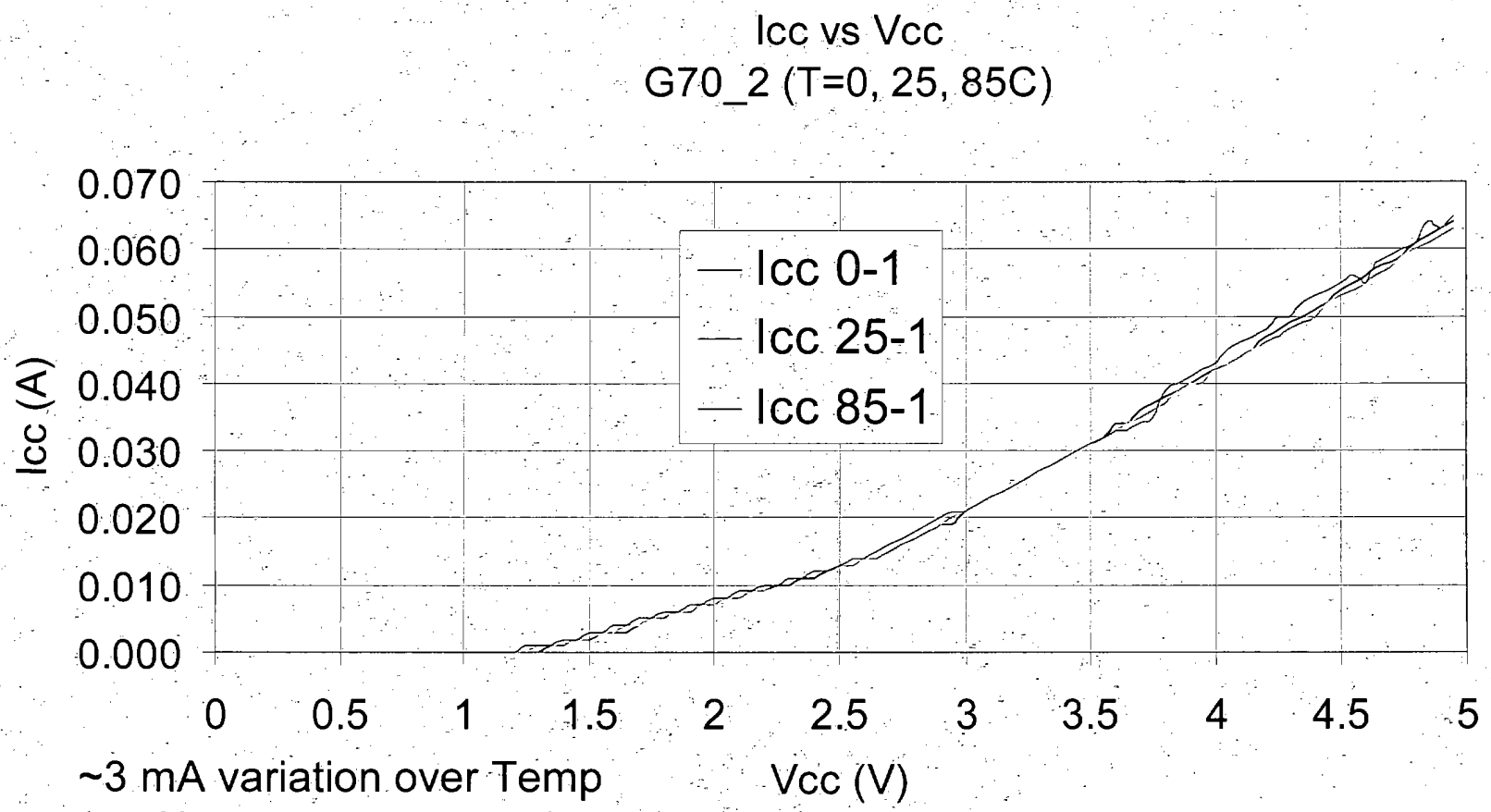

10
8
6
4
2
0
Noise Figure (dB)
No Choke (L1=0)
302
Finite Choke (L1=8nH) and R_iso = 100 ohms
304
306
Ideal Choke Inductor (L1=Infinity)
0
1
2
3
4
5
6
Frequency (GHz)

FIG. 11



~3 mA variation over Temp
(< 5% variation, T=0-85C)

~20 mA/V Vcc sensitivity

FIG. 12

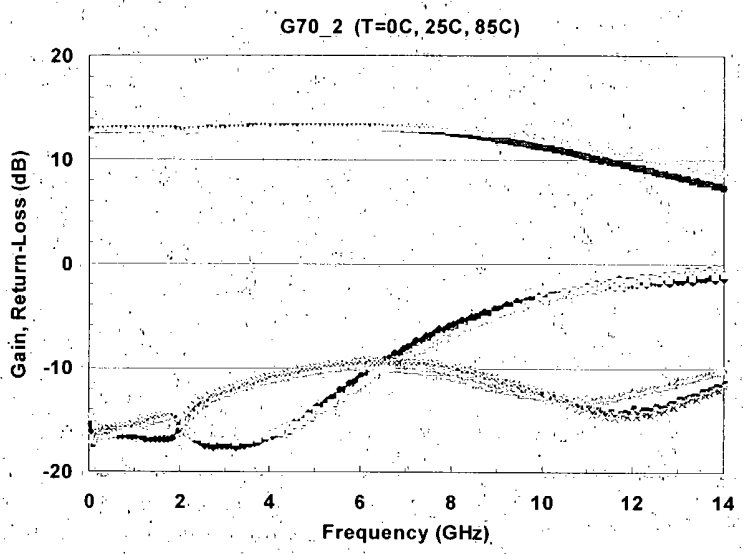
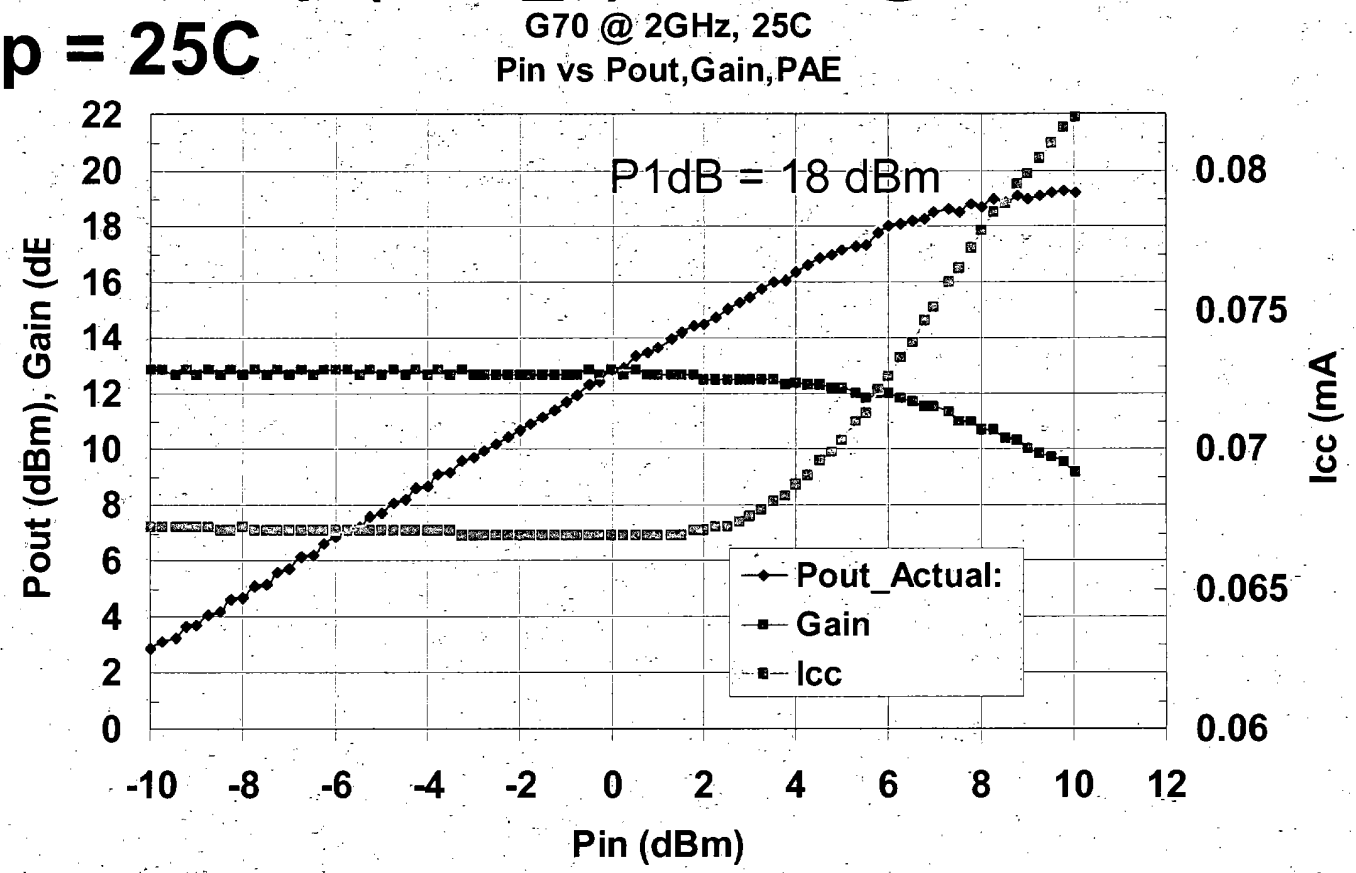

G70_2 (T=0C, 25C, 85C)
Gain, Return-Loss (dB)
20
10
0
-10
-20
0
2
4
6
8
10
12
14
Frequency (GHz)

FIG. 13

Self-bias Amp (G70_2) P1dB @ 2 GHz
Temp = 25C



Self-bias allows Icc to increase with Pin→ topology can be designed for class B,AB bias

FIG. 14